CALL FOR PANELS

DVCON US 2020

March 1-4, 2021 • Virtual

2021 DESIGN AND VERIFICATION™ DVCON CONFERENCE AND EXHIBITION UNITED STATES

DVCon US is the premier conference on the application of languages, tools and methodologies for the design and verification of electronic systems and integrated circuits. The focus of the conference is on the usage of specialized design and verification languages such as SystemVerilog, Verilog, VHDL, SystemC, PSL, and e, as well as general purpose languages such as C and C++, PERL, Tcl and Python. Tools and methodologies include the use of testbench automation, hardware-assisted verification, hardware/software co-verification, assertion-based and formal verification, transaction-level system design, high level synthesis, low power design and verification techniques, Functional Safety and Security, 3D chip designs, IP-based SoC design methods, reference flows and AMS design.

Conference attendees are primarily designers of electronic systems, ASICs and FPGAs, as well as those involved in the research, development, and application of Electronic Design Automation (EDA) tools. Presentations are highly technical in nature, and reflect real life experiences in using these languages and tools.

PANEL PROPOSAL

Deadline: September 22, 2020

Proposals: Submit online at DVCon.org.
DVCon is planning to host two highly focused panel discussions. DVCon is looking for panels that are lively, controversial, and provoke discussion on a specific topic of interest to the community. Panel sessions should not consist of paper presentations, but should have plenty of discussion engaging the audience. Panels are scheduled for 1 hour on Wednesday, March 3, 2020. Please make sure that moderator and panelists are available on Wednesday, March 3. DVCon will attempt to work with the original organizer in refining the panel, but if this is not successful, another organizer may be appointed. If multiple panel suggestions are submitted with similar topics, the committee may choose to accept one over the others, to merge the proposed panels, or to reject all of them.

TOPIC SUGGESTIONS

We invite you to contribute your knowledge and experience within the hardware design and verification, advanced tools, and new methodologies areas, and to participate in the valuable exchange of ideas. Panels should combine experiences in a given area with forward-looking statements regarding technology and industry trends, and challenges likely to be encountered as the state of the art continues to progress.

- Experiences using design and/or verification IP for System-on-Chip development
- Experiences applying machine-learning techniques
- Experiences adopting functional-safety related standards such as ISO26262, DO-254 etc.
- Design and verification sign-off and closure
- Dealing with the technical and logistical challenges of multi-site projects
- Developing, adopting and proliferating new standards
- Experiences deploying a verification methodology library, especially deployment of UVM
- Designing and/or verifying complex ASICs and FPGAs using multiple HDLs and/or HVLs in a design cycle
- Organizational and technological challenges in a pandemic
- What will our industry look like in 5-10 years given the Covid-19 disruption?

PROPOSAL SUBMISSION

Proposals should be 2-3 pages in length and should contain:

- The topic, if possible formulated as a provocative question
- The issues to be discussed, including a short listing of pro and con arguments
- Short biographies of the moderator and prospective panelists
- Any special requirements

PANEL SCHEDULE

September 22, 2020: Proposal Deadline
November 3, 2020: Accept/Reject notification
November 25, 2020: Final panel title, abstract and panelists names due for website

CONFERENCE SCHEDULE

Monday, March 1: Accellera Day Tutorials, Short Workshops, Exhibits
Tuesday, March 2: Technical Sessions, Keynote Speaker, Poster Session, Exhibit
Wednesday, March 3: Technical Sessions, Panel Discussion, Exhibits
Thursday, March 4: Tutorials, Short Workshops

For more information concerning the conference, please contact conference management:
Conference Catalysts | Laura LeBlanc | lleblanc@conferencecatalysts.com

Conference Sponsor:

accellera SYSTEMS INITIATIVE

General Chair
Aparna Dey, *Cadence Design Systems, Inc.*
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Tom Fitzpatrick, *Mentor, A Siemens Business*
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Accellera Systems Initiative is an industry consortium with a mission to provide design and verification standards required by systems, semiconductor, IP, and design tool companies to enhance a front-end design automation process. **Accellera.org**